

The leader in JTAG system test solutions

Firecron LTD
Technology Solutions

JTS06Bu

IEEE 1149.1 Gateway (Six daughter chain 8 bit)

The Ideal solution for hierarchical 1149.1 test solutions

- Device Multi-Drop Addressable via the IEEE 1149.1 protocol
- Support for 6 local scan chains addressable via the IEEE 1149.1 interface.
- Support for Pass-through™
- Support for the IEEE 1149.1 USERCODE instruction.
- Support for Status instruction enabling non-intrusive monitoring of the system card.
- Local Scan port enable signal provides the ability to use non IEEE 1149.1 compliant devices that require JTAG enable signal.
- Provides the ability to initiate Self Test on a remote PCB via a standard IEEE 1149.1 command.
- Support for JTAG Technologies AutoWR™ feature.
- Device support in all major ATPG vendors.

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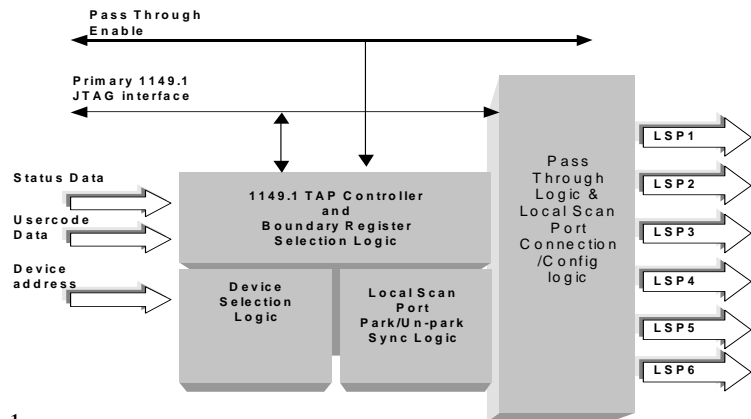


Fig. 1

Description

The JTS06BU is a one to 6 JTAG gateway, which can be partitioned via 64 separate combinations. It partitions a single JTAG chain into six separate chains. The chain can therefore be configured to operate under any combination. Controlled by software selection.

The JTS06Bu device is used to provide enhanced capabilities to the standard IEEE1149.1, it enables the IEEE1149.1 interface to be used in a true Multi-Drop environment without any additional signals. This Multi-Drop capability enables the standard IEEE1149.1 interface to be used not just for stand alone Printed Circuit Board (PCB) testing, but complete system testing including all PCB's within a system back plane environment.

The JTS06Bu also provides the capability of partitioning the PCB, into multiple smaller IEEE1149.1 scan chains totally under software control.

Partitioning the IEEE1149.1 chains on the PCB has several benefits, which include :- easier fault diagnostics capabilities as a fault on one of the IEEE1149.1 Local Scan Ports does not render the PC-testable, efficient PLD programming, faster flash programming , removal of IEEE1149.1 signal loading issues.

All of the protocols required for addressing the JTS06Bu device via the Multi-Drop capability and the protocols for configuring the which of the IEEE1149.1 Local Scan Ports (LSPs) of the JTS06Bu are to be used, is handled via the 3rd party ATPG eg Asset-Intertech and JTAG Technologies. In a Multi-Drop environment it is also possible to perform interconnect tests between multiple PCB's within the system thus extending the interconnect tests to the back plane its self.

**JTS06Bu
IEEE1149.1 JTAG**

JTS06Bu Gateway Functional Description

The basic structure of the JTS06Bu device is shown in Figure 1, the major blocks of the device are clearly identifiable. The core of the device is the 16 state IEEE1149.1 state machine, all access to the internal registers of the JTS06BU device are controlled via this state machine under normal operation as per the IEEE1149.1 Std. The address selection logic enables the JTS06Bu to operate in a Multi-drop environment within system backplane.

The selection logic compares the scanned address to the slot address value presented on the I/O of the JTS06BU device. The Local Scan Port (LSP) park / unpark logic provides control under instructions scanned in under the IEEE1149.1 protocol, to select which LSP will be placed in to the active scan chain. The pass through and LSP connection logic selects the signal paths for the LSP IEEE1149.1 signals. The device also supports a pass through mode which enables the primary IEEE1149.1 signals to be routed to any of the Local Scan Ports (LSP's). This signal routing is selectable via I/O pins on the JS06Bu device.

The JTS06Bu operation is controlled via these core blocks via three closely coupled state machines Figure 2 shows the device selection state machine, the JTS06Bu will perform an address compare on the slot address presented to the I/O of the JTS06Bu device and the value scanned in via the IEEE1149.1. If the value matches, then the JTS06Bu becomes selected and is ready for normal access via IEEE1149.1 commands. If the address does not match then the device will proceed to the unselected mode, where it will remain until the JTS06Bu is issued with the GO-TOWAIT instruction or a Reset occurs via TRST or the LSP_RESET pin.

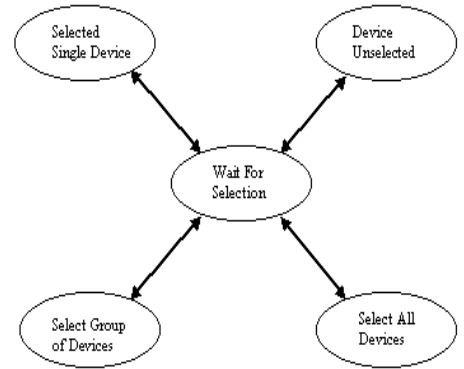


Figure 2. JTS06Bu Selection Logic State machine

The LSP Park / Unpark state machine controls the insertion of the LSP's into the current active scan chain. The ability to park the LSP in certain IEEE1149.1 states enables the JTS06Bu to perform several functions including backplane interconnect testing , IC BIST.

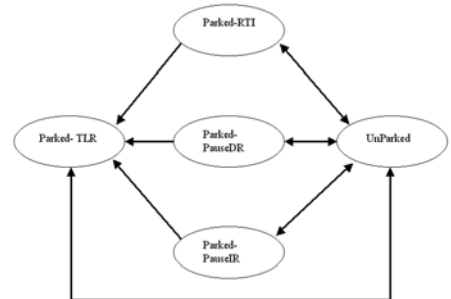


Figure 3 The Local Scan Port Park / Unpark State Machine



**JTS06Bu
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JTS06Bu Detailed Mode of Operation

**Level 1 protocol
Addressing the JTS06Bu device**

After a Test-Logic-Reset or power on the JTS06Bu device will be in its unselected mode with its TDO pin Tri-Stated, thus avoiding contention in a multi-drop environment. The JTS06Bu device responds to a device select sequence for a particular address that is auto generated in the third party test tools with respect to the address that is pre loaded set on the S(5..0) pins. Once this sequence has been completed then the JTS06Bu device is ready to respond to normal IEEE 1149.1 instructions. Note that addresses 60 through to 63 have been reserved and the JTS06Bu device will not respond if the user selects these addresses.

To be selected the JTS06Bu device should be in the wait for selection mode, which can be entered in the following manner TRST taken low to perform an asynchronous reset of the JTS06Bu device or a synchronous reset of the JTS06BU device by issuing greater than 5 TCK's when TMS is held at a logic '1' state. Finally once the device is selected then the device can be issued a GOTOWAIT instruction.

The internal IEEE1149.1 state machine of the JTS06Bu device is taken to the Shift-IR phase and the required device ID is shifted into the Instruction register. As the IEEE1149.1 state machine passes through the Update-IR phase the address is matched to the value on the S(5-0) pins on the JTS06Bu device if the values match then the device is selected and JTS06Bu device is ready to receive any normal IEEE1149.1 command.

JTS06Bu device Selection Table

S(5-0) value	IR (7 – 0) value
< 3A hex or 60 decimal	XXVVVVVV



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JTS03 Multi Cast Group selection Table

Selection Mode	Binary Address	Function
Single Address Mode	XX000000 to XX111010	Single JTS06Bu selected the TDO of the device will be active
Broad Cast Mode	XX111011	All accessible JTS06Bu devices are selected for operation, TDO on all devices will be in HighZ
Multi-Cast Group 0	XX111100	Access all JTS06Bu device that have been placed in GRP0 by their MCGR contents.
Multi-Cast Group 1	XX111101	Access all JTS06Bu device that have been placed in GRP1 by their MCGR contents.
Multi-Cast Group 2	XX111110	Access all JTS06Bu device that have been placed in GRP2 by their MCGR contents.
Multi-Cast Group 3	XX111111	Access all JTS06Bu device that have been placed in GRP3 by their MCGR contents.

JTS06Bu device Register Descrip-

Register Name	Description
Instruction Register	JTS06Bu device addressing and instruction-decode IEEE Std. 1149.1 required register
Boundary-Scan Register	IEEE Std. 1149.1 required register
Bypass Register	IEEE Std. 1149.1 required register
Device Identification Register	IEEE Std. 1149.1 optional register
User Code Register	IEEE Std. 1149.1 optional register
Status Register	JTS06Bu device non intrusive 8 bit register pre load able from the I/O pins
Self Test Register	JTS06Bu device specific single bit register for initiating self testing on a PCB
Mode Register	JTS06Bu device local-port configuration and control bits
Auto Write Register	JTS06Bu device Auto Write feature enable register
Local Scan Port Async Reset Register	JTS06Bu device Async reset register for the local scan ports



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JTS06Bu device Instruction Register OpCodes

Instructions	Hex Op-Code	Binary Op-Code	Data Register
BYPASS	FF	11111111	Bypass Register
EXTEST	00	00000000	Boundary-Scan Register
SAMPLE/PRELOAD	81	10000001	Boundary-Scan Register
IDCODE	AA	10101010	Device Identification Register
UNPARK	E7	11100111	Device Identification Register
PARKTLR	C5	11000101	Device Identification Register
PARKRTI	84	10000100	Device Identification Register
PARKPAUSE	C6	11000110	Device Identification Register
GOTOWAIT*	C3	11000011	Device Identification Register
MODESELECT	8E	10001110	Mode Register
MCGRSELECT	03	00000011	Multi-Cast Group Register.
SOFTRESET	88	10001000	Device Identification Register
USERCODE	97	10010111	User Programmable 32 Bit Identification Register
AUTOWR	98	10011000	Auto Write Feature Enable Register
STEST_PCB	99	10011001	Single bit low pulse, used to initiate function on PCB (SELF_TEST pin)
STATUS_BYTE	9A	10011010	User programmable status byte (USR_STATUS_DATA pins)
LSP_ASYNC_RESET	9B	10011011	Toggles local scan port TRST whilst maintaining the JTS06Bu in the selected state.
Other Undefined	TBD	TBD	Device Identification Register

Note: All instructions act on a single selected JTS06U device only.

* This instruction causes the JTS06U to become unselected and reverted to the Wait for address state.



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JTS06Bu device Register descriptions

Bypass Register

It is an IEEE1149.1 mandatory single bit register that can be connected between TDI and TDO of the JTS06Bu device.

Multi Cast Group Register

This 2 bit data register enables the host system to place the JTS06Bu into 1 of 4 distinct addressable groups which can be subsequently operated upon.

MCGR Register Bits [1..0]	Binary Selection Address	MCGR GROUP
00	XX111100	GRP0
01	XX111101	GRP1
10	XX111110	GRP2
11	XX111111	GRP3

Note :- The MCGR is reset to 00 upon receiving TRST or the entering of the Test-Logic-Reset state

IDCODE Register JTS06Bu

It is an optional 32 bit register that can be connected between TDI and TDO of the JTS06Bu device. The contents of the IDCODE register will be loaded with the following data when the JTS06Bu enters Test-Logic-Reset or passes through Capture-IR :-

"00000000000000001000001101101111"

Bits 1 to 11 indicate the Firecron Jedec ID value of :- "00110110111"

Bits 12 to 27 indicate the part number of the device :- "0000000000010000"

Bits 28 to 31 indicate the revision of the device :- "0000"

USRCODE Register

The USRCODE is a 8 Bit register that can be addressed via Standard IEEE1149.1 commands, which are generated by the third party test tool automatically. The end user has the ability to program the binary value that will be transmitted back to the host via the USRCODE command, by setting the binary pattern on the USRCODE pins on the JTS06Bu device. Depending on the package host silicon used, all 8 will be connected to the package, whilst the upper 24 Bits will be set to logic zero.

Note: Value is positive Logic



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SELF_TEST Register

The JTS06Bu device supports a single pin that can be controlled via the IEEE1149.1 interface. When the instruction is loaded into the the JTS06BU instruction register, a single bit data register is connected as the data register which is always reset to logic zero when the TAP state machine enters Capture-DR. This will cause the Self test pin to pulse low for 1 TCK cycle, during the Update-DR phase. This low going pulse can be used to initiate self tests on PCB's in a rack via the JTAG interface.

LSP_ASYNC_RST Register

The JTS06Bu device supports async reset tests on the devices connected in the local scan ports. The standard method of performing these test utilising the primary TRST pin is not can not be used as will cause the JTS06Bu to deselect and its internal registers to be reset. In order to enable the async reset tests on local scan ports the test tool can instruct the device to toggle the local scan port reset pins whilst maintaining the set up information in the JTS06Bu. When the instruction is loaded into the JTS06Bu instruction register, a single bit data register is connected as the data register which is always reset to logic zero when the TAP state machine enters Capture-DR. This will cause the local scan port TRST pins to pulse low for 1 TCK cycle, during the Update-DR phase.

AUTOWR Register

This is a 6 bit register that controls the passthrough of the JTAG Technologies AutoWR™ signal through to any Local Scan Port. The register is reset to all zero's on the master state machine entering the Test-Logic-Reset state.

AutoWr Register (Bit 2 – Bit 0)	Local Scan Port 3 AutoWr Signal	Local Scan Port 2 AutoWr Signal	Local Scan Port 1 AutoWr Signal
000	“Drive logic 1”	“Drive logic 1”	“Drive logic 1”
001	“Drive logic 1”	“Drive logic 1”	Active
011	“Drive logic 1”	Active	Active
100	Active	“Drive logic 1”	“Drive logic 1”
101	Active	“Drive logic 1”	Active
110	Active	Active	“Drive logic 1”
111	Active	Active	Active

Note :- The MCGR is reset to 00 upon receiving TRST or the entering of the Test-Logic-Reset state

AutoWr Register (Bit 5– Bit 3)	Local Scan Port 6 AutoWr Signal	Local Scan Port 5 AutoWr Signal	Local Scan Port 4 AutoWr Signal
000	“Drive logic 1”	“Drive logic 1”	“Drive logic 1”
001	“Drive logic 1”	“Drive logic 1”	Active
011	“Drive logic 1”	Active	Active
100	Active	“Drive logic 1”	“Drive logic 1”
101	Active	“Drive logic 1”	Active
110	Active	Active	“Drive logic 1”
111	Active	Active	Active



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MODE_SELECT Register

The Mode select register enables the many different combinations of how to connect up the local scan ports of the JTS06Bu device. A Local Scan Port is selected for connection within the scan chain by the contents of the Mode_Select register.

If the Local Scan Port is not parked in a stable state ie: Pause-DR, Pause-IR, Run-Test-Idle or Test-Logic-Reset it will be connected into the active scan chain. If all Local Scan Ports are parked in a stable state , then the JTS06Bu will perform a bypass of the 6 LSP chain section. In this way if both sections are in the bypass mode then the JTS06Bu is performing a loopback of TDI->Register->TDO to the host device.

Mode_Select Register (Bit 15 -> Bit 8)	Local Scan Port Configuration (If Port Un-parked)
XXX0X000	TDI ->Register->LSP_Data
XXX0X001	TDI ->Register->LSP1->PAD-> LSP_Data
XXX0X010	TDI ->Register->LSP2->PAD-> LSP_Data
XXX0X011	TDI ->Register->LSP1->PAD->LSP2->PAD->LSP_Data
XXX0X100	TDI ->Register->LSP3->PAD-> LSP_Data
XXX0X101	TDI ->Register->LSP1->PAD->LSP3->PAD->LSP_Data
XXX0X110	TDI ->Register->LSP2->PAD->LSP3->PAD->LSP_Data
XXX0X111	TDI ->Register->LSP1->PAD->LSP2->PAD->LSP3->PAD->LSP_Data

X = don't care

Register = JTS06Bu device instruction register or any of the JTS06Bu device test data registers.

PAD = Insertion of a 1-bit register for data synchronisation.

Upon entering Test-Logic-Reset the register bits will be loaded with 00000001

Mode_Select Register (Bit 7 -> Bit 0)	Local Scan Port Configuration (If Port Un-parked)
XXX0X000	LSP_Data ->TDO
XXX0X001	LSP_Data ->LSP4->PAD->TDO
XXX0X010	LSP_Data ->LSP5->PAD->TDO
XXX0X011	LSP_Data ->LSP4->PAD->LSP5->PAD->TDO
XXX0X100	LSP_Data ->LSP6->PAD->TDO
XXX0X101	LSP_Data ->LSP4->PAD->LSP6->PAD->TDO
XXX0X110	LSP_Data ->LSP5->PAD->LSP6->PAD->TDO
XXX0X111	LSP_Data ->LSP4->PAD->LSP5->PAD->LSP6->PAD->TDO

X = don't care

Register = JTS06Bu device instruction register or any of the JTS06Bu device test data registers.

PAD = Insertion of a 1-bit register for data synchronisation.

Upon entering Test-Logic-Reset the register bits will be loaded with 00000000



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**Passthrough Support within the
JTS06Bu Device**

The JTS06Bu device supports a Passthrough mode where the primary side master IEEE1149.1 JTAG signals can be route to any one of the Local Scan Ports. When this mode is activated the “Debug Enable” signal for that Local Scan Port will go active, which can be used to if required to place a processor such as the MPC8260 into BDM (Back Ground Debug mode). If no processors are present in the Local Scan Port, then the Passthrough mode can be used to assist in the generation of the test vectors or memory tests for the devices that are linked into the selected Local Scan Port. The Passthrough feature has the effect of simplifying the test vector generation for the Local Scan Port, as it has the effect of removing the JTS06Bu device from the test vector generation process.

Note:-

When Pass_Thru is "High" then the local scanport are under control of the JTS06BU device logic. When Pass_Thru is taken active (low) then if the LSP is not selected for communication it will pass through the primary TCK and TRST signals whilst holding TMS and TDo at logic '1'

PASS_T HRU_En able	PASS_T HRU_SE L(2)	PASS_T HRU_SE L(1)	PASS_T HRU_SE L(0)	Active Local Scan Port
High	X	X	X	Normal Opera- tion
Low	Low	Low	Low	LSP1
Low	Low	Low	High	LSP2
Low	Low	High	Low	LSP3
Low	Low	High	High	LSP4
Low	High	Low	Low	LSP5
Low	High	Low	High	LSP6



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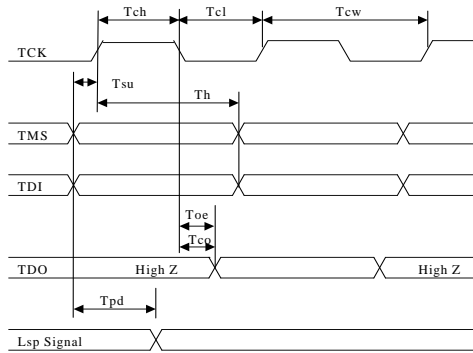
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DC Requirements

The power requirements for the JTS06Bu device are minimal and are defined within the context of this datasheet

AC Requirements

Figure 2. JTS06Bu AC Timing Diagram



SYMBOL	Parameter	MIN	MAX	UNITS
Tcw	TCK clock pulse width	100	-	nS
Tch	TCK pulse width high	50	-	nS
Tcl	TCK pulse width low	50	-	nS
Tsu	TCK Setup time	30	-	nS
Th	TCK Hold time	40	-	nS
Toe	Neg Edge TCK to valid data enable	20	-	nS
Tco	Neg Edge TCK to valid data	15	-	nS
Tpd	Pass through Mode Primary / Lsp Delay	-	10	nS



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Sup-

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port within the JTS03 Device

Absolute Maximum Ratings

Supply Voltage (Vcc) -0.3V to 5.5V
 Vi = -0.5V -20mA
 Vi = Vcc + 0.5V +20mA
 DC Input Voltage (Vi) -0.5V to Vcc +0.5V
 Input Current Iin :- 10uA

Max Junction Temperature with power applied Tj +125 degrees C

Max Storage temperature -55 to +150 degree C

Lead temperature (solder x sec)

100 LQFP
100 cBGA

Max Pkg Power Capacity @ 25C

100 LQFP
49L cBGA

ESD :

I/O

Inputs

Note. Stress above the stated maximum values may cause irreparable damage to the device, correct operation of the device at these values is not guaranteed

Recommended Operating Conditions

Supply Voltage (Vcc) 3.0V to 3.6V
 JTSXX
 Input Voltage (Vi) 0V to Vcc
 Output Voltage (Vo) 0V to Vcc
 Operating Temperature(Ta)
 Commercial 0 C to 70 C
 Industrial (Ta) -40 deg C to +85 deg C 3.0V 3.6V

DC Electrical Characteristics

Symbol	Parameter	Max	Min	Units	Condition
V _{IH}	Minimum High Input Voltage	5.25	2.0	V	
V _{IL}	Maximum Low Input Voltage	0.8V	-0.3V	V	
Symbol	Parameter	Value		Units	Condition
V _{OH}	Minimum High Output Volotage	2.4V		V	Ioh=24mA or 8mA as defined by pin
V _{OL}	Minimum Low Output Voltage	0.4V		V	Iol=24mA or 8mA as defined by pin
I _{oz}	Tristate output leakage	-10 or 10 mA		mA	
I _{cc}	Maximum quiecennt supply current	2mA		mA	
I _{ccd}	Maximum dynamic supply current	80mA			TCK freq equal to 10 Mhz



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PIN NAME	PIN TYPE	LOC 100 tqfp	LOC 100 cBGA	Description	Stable state after por/reset
LSP1_TCK	OUT	31	H4	IEEE1149.1 Test Clock on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH. Pin is PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 000,	Buffered version of signal present on primary TCK
LSP1_TMS	OUT	32	J4	IEEE1149.1 Test Mode Select on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is 0 and PASS_THRU_SEL(2:0) signals are 000,	Logic '1'
LSP1_TDO	OUT	35	H5	IEEE1149.1 Test Data Out on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 000,	Logic '1'
LSP1_TDI	IN	33	K4	IEEE1149.1 Test Data In on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 000,	
LSP1_TRST	OUT	29	K3	IEEE1149.1 Test Reset on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 000,	Buffered version of signal present on primary TRST
LSP1_AutoWR	OUT	30	J3	Flash, Memory Auto-Write on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 000 PRIM_AutoWR is routed through to pin, any other patterns on PASS_THRU_SEL(2:0) pin will drive a stable logic value.	Logic '1'
LSP1_DE	OUT	28	J2	PASS_THRU Debug Enable Output on Local Scan Port 1, active LOW when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 000 any other patterns on PASS_THRU_SEL(2:0) or PASS_THRU_ENABLE is HIGH then pin is HIGH.	Logic '1'
LSP2_TCK	OUT	41	J6	IEEE1149.1 Test Clock on Local Scan Port 2 when PASS_THRU_ENABLE is HIGH. Pin is PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 001,	Buffered version of signal present on primary TCK
LSP2_TMS	OUT	42	H6	IEEE1149.1 Test Mode Select on Local Scan Port 2 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is 0 and PASS_THRU_SEL(2:0) signals are 001,	Logic '1'
LSP2_TDO	OUT	45	J7	IEEE1149.1 Test Data Out on Local Scan Port 2 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 001,	Logic '1'

Note:

All I/O pins on the JTSxx device are pulled to logic '1' by internal active pullups. The typical value of the pull up is between 50K-.70K Ohms. When the JTSxx when is the HighZ state (ie TOE pin taken to logic '0') the device's own boundary scan IEEE1149.1 Test Access Port (TAP) can still be accessed and the device's I/O pins will drive if enabled by the Extst



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PIN NAME	PIN TYPE	LOC 100 tqfp	LOC 100 cBGA	Description	Stable state after por/reset
LSP2_TDI	IN	44	K7	IEEE1149.1 Test Data In on Local Scan Port 2 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 001,	
LSP2_TRST	OUT	37	K5	IEEE1149.1 Test Reset on Local Scan Port 2 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 001,	Buffered version of signal present on primary TRST
LSP2_AutoWR	OUT	40	K6	Flash, Memory Auto-Write on Local Scan Port 2 when PASS_THRU_ENABLE is HIGH, when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 001 PRIM_AutoWR is routed through to pin, any other patterns on PASS_THRU_SEL(2:0) pin will drive a stable logic value.	Logic '1'
LSP2_DE	OUT	36	J5	PASS_THRU Debug Enable Output on Local Scan Port 2, active LOW when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 001 any other patterns on PASS_THRU_SEL(2:0) or PASS_THRU_ENABLE is HIGH then pin is HIGH.	Logic '1'
LSP3_TCK	OUT	49	K9	IEEE1149.1 Test Clock on Local Scan Port 3 when PASS_THRU_ENABLE is HIGH. Pin is PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 010,	Buffered version of signal present on primary TCK
LSP3_TMS	OUT	50	K10	IEEE1149.1 Test Mode Select on Local Scan Port 3 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is 0 and PASS_THRU_SEL(2:0) signals are 010,	Logic '1'
LSP3_TDO	OUT	53	H10	IEEE1149.1 Test Data Out on Local Scan Port 3 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 010,	Logic '1'
LSP3_TDI	IN	52	J10	IEEE1149.1 Test Data In on Local Scan Port 3 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 010,	
LSP3_TRST	OUT	47	J8	IEEE1149.1 Test Reset on Local Scan Port 3 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 010,	Buffered version of signal present on primary TRST
LSP3_LSP_AutoWR	OUT	48	K8	Flash, Memory Auto-Write on Local Scan Port 3 when PASS_THRU_ENABLE is HIGH, when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 010 PRIM_AutoWR routed through to pin, any other patterns on PASS_THRU_SEL(2:0) pin will drive a stable logic value.	Logic '1'
LSP3_DE	OUT	46	H7	PASS_THRU Debug Enable Output on Local Scan Port 3, active LOW when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 010 any other patterns on PASS_THRU_SEL(2:0) or PASS_THRU_ENABLE is HIGH then pin is HIGH.	Logic '1'

Note:

All I/O pins on the JTSxx device are pulled to logic '1' by internal active pullups. The typical value of the pull up is between 50K-.70K Ohms. When the JTSxx when is the HighZ state (ie TOE pin taken to logic '0') the device's own boundary scan IEEE1149.1 Test Access Port (TAP) can still be accessed and the device's I/O pins will drive if enabled by the Exttest



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JTS06Bu
IEEE1149.1 JTAG

PIN NAME	PIN TYPE	LOC 100 tqfp	LOC 100 cBGA	Description	Stable state after por/reset
LSP4_TCK	OUT	79	A8	IEEE1149.1 Test Clock on Local Scan Port 4 when PASS_THRU_ENABLE is HIGH. Pin is PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 011,	Buffered version of signal present on primary TCK
LSP4_TMS	OUT	78	A9	IEEE1149.1 Test Mode Select on Local Scan Port 4 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is 0 and PASS_THRU_SEL(2:0) signals are 011,	Logic '1'
LSP4_TDO	OUT	76	B10	IEEE1149.1 Test Data Out on Local Scan Port 4 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 011,	Logic '1'
LSP4_TDI	IN	77	B9	IEEE1149.1 Test Data In on Local Scan Port 4 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 011,	
LSP4_TRST	OUT	81	A7	IEEE1149.1 Test Reset on Local Scan Port 4 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 011,	Buffered version of signal present on primary
LSP4_AutoWR	OUT	80	B8	Flash, Memory Auto-Write on Local Scan Port 4 when PASS_THRU_ENABLE is HIGH, when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 011 PRIM_AutoWR is routed through to pin, any other patterns on PASS_THRU_SEL(2:0) pin is will drive a stable logic value.	Logic '1'
LSP4_DE	OUT	83	B7	PASS_THRU Debug Enable Output on Local Scan Port 4, active LOW when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 011 any other patterns on PASS_THRU_SEL(2:0) or PASS_THRU_ENABLE is HIGH then pin is HIGH.	Logic '1'
LSP5_TCK	OUT	70	D10	IEEE1149.1 Test Clock on Local Scan Port 5 when PASS_THRU_ENABLE is HIGH. Pin is PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 100,	Buffered version of signal present on primary TCK
LSP5_TMS	OUT	69	D9	IEEE1149.1 Test Mode Select on Local Scan Port 5 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is 0 and PASS_THRU_SEL(2:0) signals are 100,	Logic '1'
LSP5_TDO	OUT	67	E8	IEEE1149.1 Test Data Out on Local Scan Port 5 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 100,	Logic '1'
LSP5_TDI	IN	68	E7	IEEE1149.1 Test Data In on Local Scan Port 5 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 100,	
LSP5_TRST	OUT	72	C9	IEEE1149.1 Test Reset on Local Scan Port 5 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 100,	Buffered version of signal present on primary
LSP5_AutoWR	OUT	71	D8	Flash, Memory Auto-Write on Local Scan Port 5 when PASS_THRU_ENABLE is HIGH, when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 100 PRIM_AutoWR is routed through to pin, any other patterns on PASS_THRU_SEL(2:0) pin is will drive a stable logic value.	Logic '1'
LSP5_DE		75	C10	PASS_THRU Debug Enable Output on Local Scan Port 5, active LOW when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 100 any other patterns on PASS_THRU_SEL(2:0) or PASS_THRU_ENABLE is HIGH then pin is HIGH.	Logic '1'

Note:

All I/O pins on the JTSxx device are pulled to logic '1' by internal active pullups. The typical value of the pull up is between 50K-.70K Ohms. When the JTSxx when is the HighZ state (ie TOE pin taken to logic '0') the device's own boundary scan IEEE1149.1 Test Access Port (TAP) can still be accessed and the device's I/O pins will drive if enabled by the Exttest



JTS06Bu
IEEE1149.1 JTAG

PIN NAME	PIN TYPE	LOC 100 tqfp	LOC 100 eBGA	Description	Stable state after por/reset
LSP6_TCK	OUT	61	F10	IEEE1149.1 Test Clock on Local Scan Port 6 when PASS_THRU_ENABLE is HIGH. Pin is PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 101,	Buffered version of signal present on primary TCK
LSP6_TMS	OUT	60	F9	IEEE1149.1 Test Mode Select on Local Scan Port 6 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is 0 and PASS_THRU_SEL(2:0) signals are 101,	Logic '1'
LSP6_TDO	OUT	57	G10	IEEE1149.1 Test Data Out on Local Scan Port 6 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 101,	Logic '1'
LSP6_TDI	IN	58	G8	IEEE1149.1 Test Data In on Local Scan Port 6 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 101,	
LSP6_TRST	OUT	64	E9	IEEE1149.1 Test Reset on Local Scan Port 5 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 101,	Buffered version of signal present on
LSP6_AutoWR	OUT	63	F7	Flash, Memory Auto-Write on Local Scan Port 6 when PASS_THRU_ENABLE is HIGH, when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 101 PRIM_AutoWR is routed through to pin, any other patterns on PASS_THRU_SEL(2:0) pin is will drive a stable logic value.	Logic '1'
LSP6_DE	OUT	65	E10	PASS_THRU Debug Enable Output on Local Scan Port 6, active LOW when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(2:0) signals are 101 any other patterns on PASS_THRU_SEL(2:0) or PASS_THRU_ENABLE is HIGH then pin is HIGH.	Logic '1'
PRIM_TCK	IN	87	A6	IEEE1149.1 Primary Test Clock Input	
PRIM_TMS	IN	21	G2	IEEE1149.1 Primary Test Mode Select Input	
PRIM_TDO	OUT	20	G1	IEEE1149.1 Primary Test Data Output, TRI-STATE when	HighZ
PRIM_TDI	IN	19	G3	IEEE1149.1 Primary Test Data Input	
PRIM_TRST	IN	22	H2	IEEE1149.1 Primary Test Reset Input, active LOW asynchronous reset of JTS06, deselecting the JTS06 and placing the	
PRIM_AutoWR	IN	16	F1	Primary Auto-Write Input controlled by test equipment to shorten Flash memory programming	
S(0)	IN	99	A2	JTS06Bu Slot Address(5:0) inputs, used to set address at which JTS06Bu will respond, typically set by hardwired	
S(1)	IN	100	B2		
S(2)	IN	5	C2		
S(3)	IN	6	D3		
S(4)	IN	7	D1		
S(5)	IN	8	D2		

Note:

All I/O pins on the JTSxx device are pulled to logic '1' by internal active pullups. The typical value of the pull up is between 50K-.70K Ohms. When the JTSxx when is the HighZ state (ie TOE pin taken to logic '0') the device's own boundary scan IEEE1149.1 Test Access Port (TAP) can still be accessed and the device's I/O pins will drive if enabled by the Exttest



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IEEE1149.1 JTAG

PIN NAME	PIN TYPE	LOC 100 tqfp	LOC 100 eBGA	Description	Stable state after por/reset
*TOE	IN	88	B6	Test Output Enable Input TRI-STATES all local scan ports, when taken to a logic low.	
LSP_RESET_n	IN	14	F4	Local Scan Port Reset input, active LOW resets JTS06 to GOTOWAIT and pulses all LSP TRST pins LOW to reset all devices with TRST function, typically this signal would be connected to a power on reset function.	
JTS06_SELECTED	OUT	25	K1	JTS06Bu_selected Output, active LOW when JTS06 is selected, typically used to control off board buffering.	Logic '1'
LSP_ENABLE	OUT	24	J1	Local Scan Port enabled active LOW Output when JTS06BU is selected and in level 1 protocol, typically used to set IEEE1149.1	Logic '1'
USR_STATUS_BYTE(7:0)	IN	84, 85, 92, 93, 94, 96, 97, 98 (MSB -LSB)	C7,C6,C5,C4, B4,A4,B3,A3 (MSB-LSB)	JTS06Bu Status Byte inputs (7:0), are used to provide status information of the PCB under test back to the test master via the IEEE1149.1 bus ie:- Eight signals levels can be monitored and then reported via the IEEE1149.1 bus in a non intrusive manner.	
SELF_TEST	OUT	27	K2	Provides a low going pulse under command from the IEEE1149.1 bus which can be used to start self test functions on a PCB	Logic '1'
PASS_THRU_Enable	IN	9	E4	PASS_THRU enable Input active HIGH disables PASS_THRU function, active LOW enables PASS_THRU mode.	
PASS_THRU_SEL(2:0)	IN	13,12,10 (MSB-LSB)	E2,E1,E3 (MSB-LSB)	JTS06Bu PASS_THRU select inputs (2:0), used to select active routing of PASS_THRU port enabled by active LOW on PASS_THRU_Enable pin. 000 = LSP1, 001 = LSP2, 010 = LSP3, 011 = LSP4, 100 = LSP5, 101 = LSP6	
GND	POWER	38, 86, 11, 26, 43, 59, 74, 95, 2, 17, 54, 55 90	D6, G5, C3, D7, E5, F6, G4,H8, H9, J9,B1, A5, F2	JTS06Bu Ground connection	
VCC	POWER	39, 91, 3, 18, 34, 51, 66, 82,23,56	D5, G6, C8, D4, E6, F5, G7, H3,G9,H1	JTS06Bu VCC connection	

Note:

All I/O pins on the JTSxx device are pulled to logic '1' by internal active pullups. The typical value of the pull up is between 50K-.70K Ohms. When the JTSxx when is the HighZ state (ie TOE pin taken to logic '0') the device's own boundary scan IEEE1149.1 Test Access Port (TAP) can still be accessed and the device's I/O pins will drive if enabled by the Exttest



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JTS06Bu
IEEE1149.1 JTAG

PIN NAME	PIN TYPE	LOC 100 tqfp	LOC 100 cBGA	Description	Stable state after por/reset
ASIC_TEST_EN	No Connect	89	B5	Factory test enable pin, this pin should be left un connected.	
ASIC_TCK	IN	62	F8	IEEE1149.1 ASIC Test Clock Input	
ASIC_TMS	IN	15	F3	IEEE1149.1 ASIC Test Mode Select Input	
ASIC_TDO	OUT	73	A10	IEEE1149.1 ASIC Test Clock Output	
ASIC_TDI	IN	4	A1	IEEE1149.1 ASIC Test Clock Input	
No Connects		1	C1		

Mechanical Requirements

This is a 100 pin plastic TQFP (Thin Quad Flat Pack) package

Leadframe Plating: Copper base material with a 5-micron (200 micro-inches) minimum of Tin/Lead overplating containing 10 - 40% lead.

Terminations:

Coplanarity (from component seating plane): 0.1 mm (0.004 inches) max.

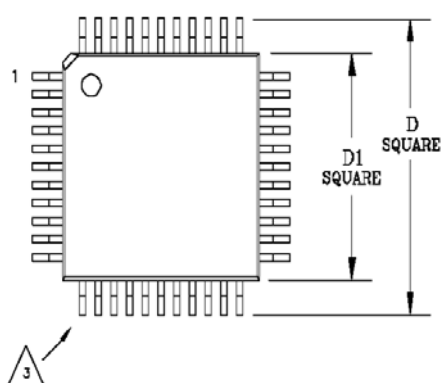
Seating plane is the plane established by the contact points of three or more leads that support the part when it is placed on top of a planar surface. Deviation from coplanarity is the distance between the intended contact point of a lead and the established seating plane per JESD22-B108.

Lead Skew: Perpendicularity of the lead rows with respect to reference axes created by the center leads of each row to be within 0.05 mm (0.002 inches). Also, the lead position is to be within 0.2 mm (0.008 inches) with respect to the reference axis.

Leaded Parts shall comply with the test method appropriate to this part in JESD22-B102.

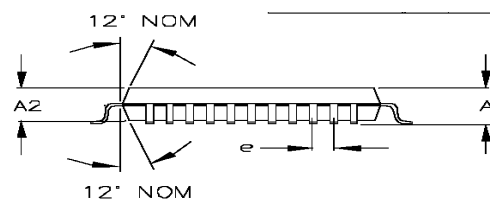
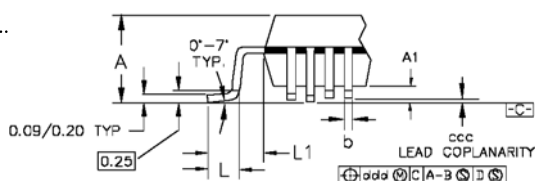
Solderability Test Method.

IC Package Configuration:



SYMBOL	TOL	LEADS	100 LEAD
A	MAX.		1.60
A1	MIN \ NAX		0.05 \ 0.15
A2	MIN \ NOM \ MAX		1.35 \ 1.40 \ 1.45
D	BASIC		16.00
D1	BASIC		14.00
L	±0.15		0.60
L1	REF		1.00
b	MIN \ MAX		0.17 \ 0.27
e	BASIC		0.50
ccc	MAX		0.08
ddd	NOM		0.08
JEDEC REF #			MS-026

NOTES:
1. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
2. PLASTIC BODY DIMENSIONS DO NOT INCLUDE FLASH OR PROTRUSION.
3. MAX ALLOWABLE 0.85 PER SIDE.
4. LEAD COUNT ON DRAWING NOT REPRESENTATIVE OF ACTUAL PACKAGE.



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Controller

BGA Package information

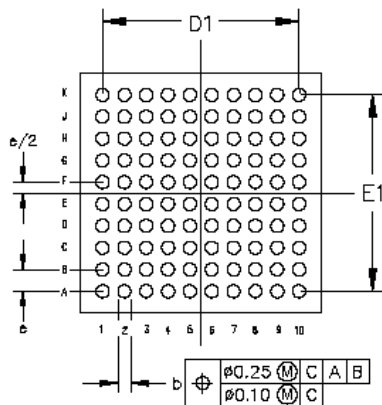
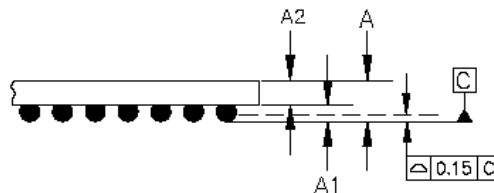
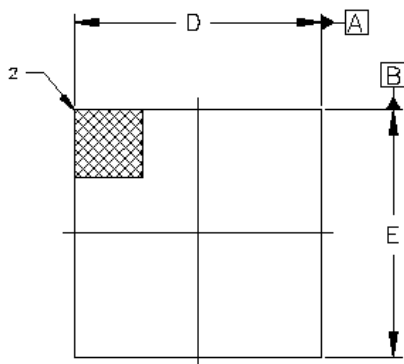
Mechanical Requirements

This is a 100 pin plastic cBGA (Ball grid array) package

Leaded Parts shall comply with the test method appropriate to this part in JESD22-B102,

Solderability Test Method.

IC Package Configuration:



SYMBOL	DIMENSIONS		
	MIN.	NOM.	MAX.
A	—	—	1.20
A1	0.30	—	—
A2	0.25	—	1.10
B	0.60	0.60	0.70
D	11.00 BSC		
D1	9.00 BSC		
E	11.00 BSC		
E1	8.00 BSC		
d	1.00		
PACKAGE NUMBER	FBGA100-11F		
JEDDEC REF #	MO-102 VAR. 092-1		

NOTES
 1. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
 2. DETAILS OF PL COORDS ARE OPTIONAL, AND MAY CONSIST OF INC. DOT, LASER MARK, OR METALLIC IMPRINT, BUT MUST BE LOCATED WITHIN THE SOLID BOUNDED.



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Device Selector Guide

JTS06BU-10LT100IG

Family:	LSP Ports	Speed grade	Package:	Pin count:	Extentions
JTS	2	10 Mhz	LT: LQFP	32	G: Green and RoHS
JTL	5	30 MHz	F: BGA	38	
JTX	7	50 Mhz	QN: QFN	100	Blank Leded
	9			144	
				176	
				208	
				256	I: industrial
					Blank: Commer- cial

JTS Device family

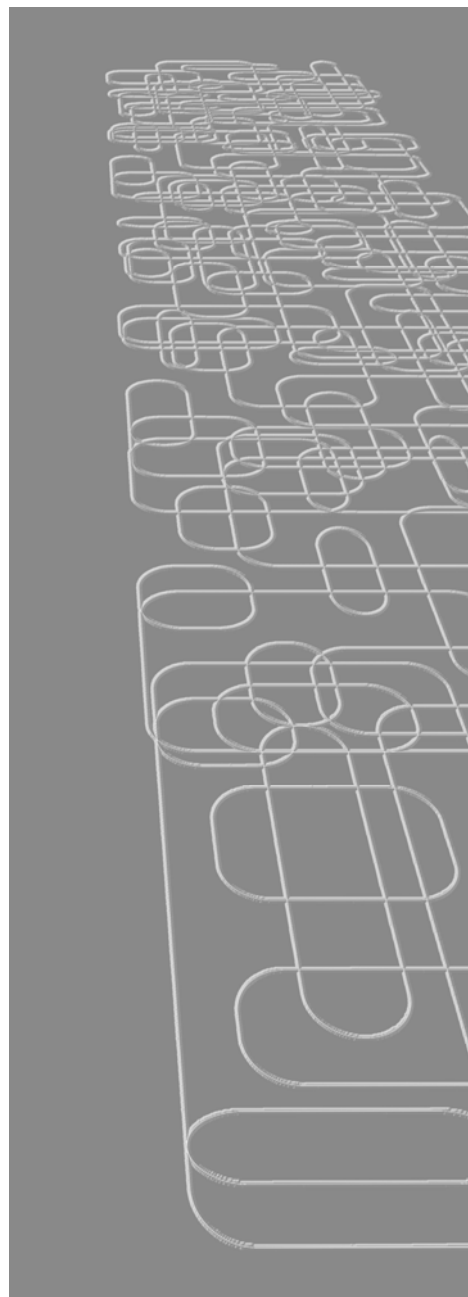
Device Mas- ter	Description	Package Options				
		49CB GA	100 cBGA (1mm pitch)	100 TQFP	144 cBGA (1mm pitch)	256 fBGA (1mm pitch)
JTS01	Controller		X	X		
JTS02	Sequencer		X	X		
JTS03U	3 Port Gateway (16 bit usercode)		X	X		
JTS06Bu	6 Port Gateway (8 bit status/usercode)		X	X		
JTS10U	6 Port Gateway (16 bit usercode) + Controller				X	



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JTS06Bu

IEEE1149.1 JTAG



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A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness

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