The leader in JTAG system test solutions

Firecron LTD
Technology Solutions

JTS03U

IEEE 1149.1 Gateway (Three daughter chain)

The Ideal solution for hiarachical 1149.1 test solutions

- **Device Multi-Drop Addressable via the IEEE 1149.1 protocol**
- **Support for 3 local scan chains addressable via the IEEE 1149.1 interface.**
- **Support for Pass-through**ä
- **Support for the IEEE 1149.1 USERCODE instruction.**
- **Support for Status instruction enabling non-intrusive monitoring of the system card.**
- **Local Scan port enable signal provides the ability to use non IEEE 1149.1 compliant devices that require JTAG enable signal.**
- **Provides the ability to initiate Self Test on a remote PCB via a standard IEEE 1149.1 command.**
- **Support for JTAG Technologies AutoWR**ä **feature.**
- **Device support in all major ATPG vendors**

Firecron LTD
Devonshire House,
66 Church Street,
Surrey KT22 8DP.

Phone: 00 44 (0)1372 477127
Fax: 00 44 (0)1372 477128
Email: Sales@firecron.com

Web site : WWW.Firecron.com

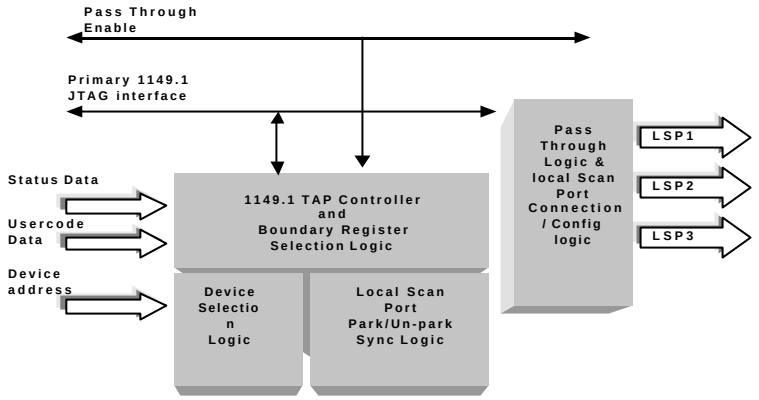


Fig. 1

Description

The JTS03U is a one to 3-port JTAG gateway, which can be partitioned via 8 separate combinations. It partitions a single JTAG chain into three separate chains. The chain can therefore be configured to operate under any combination. Controlled by software selection.

The JTS03U device is used to provide enhanced capabilities to the standard IEEE1149.1. It enables the IEEE1149.1 interface to be used in a true Multi-Drop environment without any additional signals. This Multi-Drop capability enables the standard IEEE1149.1 interface to be used not just for stand alone Printed Circuit Board (PCB) testing, but complete system testing including all PCBs within a system back plane environment.

The JTS03U also provides the capability of partitioning the PCB, into multiple smaller IEEE1149.1 scan chains totally under software control.

Partitioning the IEEE1149.1 chains on the PCB has several benefits, which include :- easier fault diagnostics capabilities, as a fault on one of the IEEE1149.1 Local Scan Ports does not render the PCB un-testable, efficient PLD programming, faster flash programming ,removal of IEEE1149.1 signal loading issues.

All of the protocols required for addressing the JTS03U device via the Multi-Drop capability and the protocols for configuring the which of the IEEE1149.1 Local Scan Ports (LSPs) of the JTS03U are to be used , is handled via the 3rd party ATPG eg Asset-Intertech and JTAG Technologies. In a Multi-Drop environment it is also possible to perform interconnect tests between multiple PCBs within the system thus extending the interconnect tests to the back plane its self.

The Leader in IEEE 1149.1 Design for Test Solutions

JTS03U
IEEE1149.1 JTAG
3 Port Gateway

JTS03U Gateway Functional Description

The basic structure of the JTS03U device is shown in Figure 1. The major blocks of the device are clearly identifiable. The core of the device is the 16 state IEEE1149.1 state machine, all access to the internal registers of the JTS03U device are controlled via this state machine under normal operation as per the IEEE1149.1 Std. The address selection logic enables the JTS03U to operate in a Multi-drop environment within system backplane.

The address selection logic compares the scanned address to the slot address value presented on the I/O of the JTS03U device. The Local Scan Port (LSP) park / unpark logic provides control through instructions scanned in under the IEEE1149.1 protocol, to select which LSP will be placed in to the active scan chain. The pass through and LSP connection logic selects the signal paths for the LSP IEEE1149.1 signals. The device also supports a pass through mode which enables the primary IEEE1149.1 signals to be routed to any of the Local Scan Ports (LSP's). This signal routing is selectable via I/O pins on the JS03U device.

The JTS03U operation is controlled via core blocks, through three closely coupled state machines Figure 2 shows the device selection state machine. The JTS03U will perform an address compare on the slot address presented at its I/O of the JTS03U device and the value scanned in via the IEEE1149.1. If the value matches, then the JTS03U becomes selected and is ready for normal access via IEEE1149.1 commands. If the address does not match then the device will proceed to the unselected mode, where it will remain until the JTS03U is issued with the GO-TOWAIT instruction or a Reset occurs via TRST or the LSP_RESET pin.

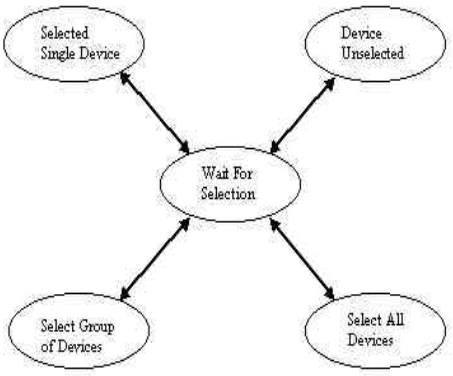


Figure 2. JTS03U Selection Logic State machine

The LSP Park / Unpark state machine controls the insertion of the LSP's into the current active scan chain. The ability to park the LSP in certain IEEE1149.1 states enables the JTS03U to perform several functions including backplane interconnect testing , IC BIST.

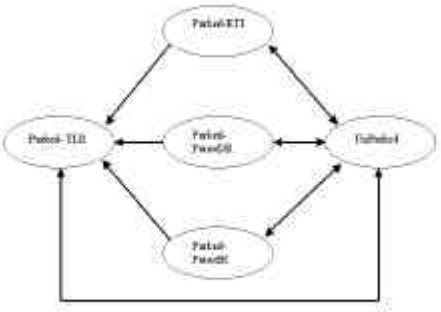


Figure 3 The Local Scan Port Park / Unpark State Machine

JTS03U
IEEE1149.1 JTAG
3 Port Gateway

JTS03U Detailed Mode of Operation

Level 1 protocol
Addressing the JTS03U device

After a Test-Logic-Reset or power on, the JTS03U device is in its unselected mode with its TDO pin Tri-Stated, thus avoiding contention in a multi-drop environment.

The JTS03U device will respond to a device select sequence for a particular address that is auto generated in the third party test tools with respect to the address that is pre loaded set on the S(5..0) pins. Once this sequence has been completed, the JTS03U device is ready to respond to normal IEEE 1149.1 instructions. It must be noted that addresses 60 through to 63 have been reserved and the JTS03U device will not respond if the user selects these addresses.

To be selected , the JTS03U device should be in the wait-for-selection mode which can be entered in to by issuing an asynchronous reset (through the deassertion of TRST) or via a synchronous reset by issuing greater than 5 TCK's when TMS is held at a logic '1' state are which the device is selected. After the device has been selected, it can be issued a GOTOWAIT instruction.

The internal IEE1149.1 state machine of the JTS03U device is taken to the Shift-IR phase and the required. Device ID is shifted into the Instruction register. As the IEEE1149.1 state machine passes through the Update-IR phase, the address is matched to the value on the S(5-0) pins on the JTS03U device; if the values match then the device is selected and JTS03U device is ready to receive any normal IEEE1149.1 command.

JTS03U device Selection Table

S(5-0) value	IR (7 – 0) value
< 3A hex or 60 decimal	XXVVVVVV

JTS03U
IEEE1149.1 JTAG
3 Port Gateway

JTS03 Multi Cast Group selection Table

Selection Mode	Binary Address	Function
Single Address Mode	XX000000 to XX111010	Single JTS03U selected the TDO of the device will be active
Broad Cast Mode	XX111011	All accessable JTS03U devices are selected for operation, TDO on all devices will be in HighZ
Multi-Cast Group 0	XX111100	Access all JTS03U device that have been placed in GRP0 by their MCGR contents.
Multi-Cast Group 1	XX111101	Access all JTS03U device that have been placed in GRP1 by their MCGR contents.
Multi-Cast Group 2	XX111110	Access all JTS03U device that have been placed in GRP2 by their MCGR contents.
Multi-Cast Group 3	XX111111	Access all JTS03U device that have been placed in GRP3 by their MCGR contents.

JTS03U device Register Description

Register Name	Description
Instruction Register	JTS03U device addressing and instruction-decode IEEE Std. 1149.1 required register
Boundary-Scan Register	IEEE Std. 1149.1 required register
Bypass Register	IEEE Std. 1149.1 required register
Device Identification Register	IEEE Std. 1149.1 optional register
User Code Register	IEEE Std. 1149.1 optional register
Status Register	JTS03U device non intrusive 8 bit register pre load able from the I/O pins
Self Test Register	JTS03U device specific single bit register for initiating self testing on a PCB
Mode Register	JTS03U device local-port configuration and control bits
Auto Write Register	JTS03U device Auto Write feature enable register
Local Scan Port Async Reset Register	JTS03U device Async reset register for the local scan ports

JTS03U
IEEE1149.1 JTAG
3 Port Gateway

JTS03U device Instruction Register OpCodes

Instructions	Hex Op-Code	Binary Op-Code	Data Register
BYPASS	FF	11111111	Bypass Register
EXTEST	00	00000000	Boundary-Scan Register
SAMPLE/PRELOAD	81	10000001	Boundary-Scan Register
IDCODE	AA	10101010	Device Identification Register
UNPARK	E7	11100111	Device Identification Register
PARKTLR	C5	11000101	Device Identification Register
PARKRTI	84	10000100	Device Identification Register
PARKPAUSE	C6	11000110	Device Identification Register
GOTOWAIT*	C3	11000011	Device Identification Register
MODESELECT	8E	10001110	Mode Register
MCGRSELECT	03	00000011	Multi-Cast Group Register.
SOFTRESET	88	10001000	Device Identification Register
USERCODE	97	10010111	User Programable 16 Bit Identi-fication Register
AUTOWR	98	10011000	Auto Write Feature Enable Register
STEST_PCB	99	10011001	Single bit low pulse, used to initiate function on PCB (SELF_TEST pin)
STATUS_BYTE	9A	10011010	User programmable status byte (USR_STATUS_DATA pins)
LSP_ASYNC_RESET	9B	10011011	Toggles local scan port TRST whilst maintaining the JTS03U in the selected state.
Other Undefined	TBD	TBD	Device Identification Register

Note: All instructions act on a single selected JTS03U device only.

* This instruction causes the JTS03U to become unselected and reverted to the Wait for address state.

JTS03U device Register descriptions

Bypass Register

It is a mandatory single bit register that can be connected between TDI and TDO of the JTS03U device.

Multi Cast Group Register

This 2 bit data register enables the host system to place the JTS03U into 1 of 4 distinct addressable groups which can be subsequently operated upon.

MCGR Register Bits [1..0]	Binary Selection Address	MCGR GROUP
00	XX111100	GRP0
01	XX111101	GRP1
10	XX111110	GRP2
11	XX111111	GRP3

Note :- The MCGR is reset to 00 upon receiving TRST or the entering of the Test-Logic-Reset state

IDCODE Register

It is an optional 32 bit register that can be connected between TDI and TDO of the JTS03U device. The contents of the IDCODE register will be loaded with the following data when the JTS03U enters Test-Logic-Reset or passes through Capture-IR :-

"00000000000000001000001101101111"

Bits 1 to 11 indicate the Firecron Jedec ID value of :- “00110110111”
Bits 12 to 27 indicate the part number of the device :- “0000000000001000”
Bits 28 to 31 indicate the revision of the device :- “0000”

USRCODE Register on the JTS03U device

The USRCODE is a 32 Bit register that can be addressed via Standard IEEE1149.1 commands, which are generated by the third party test tool automatically. The end user has the ability to program the binary value that will be transmitted back to the host via the USRCODE command; by setting the binary pattern on the USRCODE pins on the JTS03U device. Depending on the package host silicon used, either all 32 Bits or the least significant 16Bits will be connected to the package, whilst the upper 16 Bits will be set to logic zero.
Note: Value is positive Logic

STATUS_BYTE Register

The STATUS_BYTE Register on the JTS03U device provides an means to sense the value on the USR_STATUS_DATA pins on the JTS03U device. This is an 8-bit field where the user can non-intrusively monitor signals on the PCB via the IEEE1149.1 interface. The data in the register is loaded each time the state machine passes through the Capture-DR phase.
Note: Value is positive Logic

SELF_TEST Register

The JTS03U device supports a single pin that can be controlled via the IEEE1149.1 interface. When the instruction is loaded into the the JTS03U instruction register, a single bit data register is connected as the data register which is always reset to logic zero when the TAP state machine enters Capture-DR. This will cause the Self test pin to pulse low for 1 TCK cycle, during the Update-DR phase. This low going pulse can be used to initiate self tests on PCB's in a rack via the JTAG interface.

LSP_ASYNC_RST Register

The JTS03U device supports async reset tests on the devices connected in the local scan ports. The standard method of performing these test utilising the primary TRST pin is not can not be used as will cause the JTS03U to deselect and its internal registers to be reset. In order to enable the async reset tests on local scan ports the test tool can instruct the device to toggle the local scan port reset pins whilst maintaining the set up information in the JTS03U. So that when the instruction is loaded into the JTS03U instruction register, a single bit data register is connected as the data register which is always reset to logic zero when the TAP state machine enters Capture-DR. This will cause the local scan port TRST pins to pulse low for 1 TCK cycle, during the Update-DR phase.

AUTOWR Register on the JTS03U device

This is a 3 bit register that controls the passthrough of the JTAG Technologies AutoWR™ signal through to any Local Scan Port. The register is reset to all zero's on the master state machine entering the Test-Logic-Reset state.

AutoWr Register (Bit 2 – Bit 0)	Local Scan Port 3 AutoWr Signal	Local Scan Port 2 AutoWr Signal	Local Scan Port 1 AutoWr Signal
000	High Z	High Z	High Z
001	High Z	High Z	Active
011	High Z	Active	Active
100	Active	High Z	High Z
101	Active	High Z	Active
110	Active	Active	High Z
111	Active	Active	Active

MODE_SELECT Register on the JTS03U device

The Mode select register allows the LSP of the JTS03U to be connected in the various different configurations. The Local Scan Port is selected for connection within the scan chain by the contents of the Mode_Select register. If the Local Scan Port is not parked in a stable state ie: Pause-DR, Pause-IR, Run-Test-Idle or Test-Logic-Reset it will be connected into the active scan chain. If all Local Scan Ports are parked in a stable state , then the JTS03U will perform loop back of TDI->Register->TDO.

Mode_Select Register (Bit 7 -> Bit 0)	Local Scan Port Configuration (If Port Unparked)
XXX0X000	TDI ->Register->TDO
XXX0X001	TDI ->Register->LSP1->PAD->TDO
XXX0X010	TDI ->Register->LSP2->PAD->TDO
XXX0X011	TDI ->Register->LSP1->PAD->LSP2->PAD->TDO
XXX0X100	TDI ->Register->LSP3->PAD->TDO
XXX0X101	TDI ->Register->LSP1->PAD->LSP3->PAD->TDO
XXX0X110	TDI ->Register->LSP2->PAD->LSP3->PAD->TDO
XXX0X111	TDI ->Register->LSP1->PAD->LSP2->PAD->LSP3->PAD->TDO

MODE_SELECT Register on the JTS03U device

The Mode select register enables the many different combinations of how to connect up the local scan ports of the JTS03U device. If a Local Scan Port is selected for connection within the scan chain by the

Passthrough Support within the JTS03U Device

The JTS03U device supports a Passthrough mode where the primary side or master IEEE1149.1 JTAG signals can be routed to any one of the Local Scan Ports. When this mode is activated the "Debug Enable" signal for that Local Scan Port will go active, which can be used to if required to place a processor such as the MPC8260 into BDM (Back Ground Debug mode). If no processors are present in the Local Scan Port, then the Passthrough mode can be used to assist in the generation of the test vectors or memory tests for the devices that are linked into the selected Local Scan Port.

The Passthrough feature has the effect of simplifying the test vector generation for the Local Scan Port, as it has the effect of removing the JTS03U device from the test vector generation process.

PASS_THRU_ENABLE	PASS_THRU_SEL(1)	PASS_THRU_SEL(0)	Active Local Scan Port
High	X	X	Normal Operation
Low	low	Low	LSP1
Low	Low	High	LSP2
Low	High	Low	LSP3

Note:-

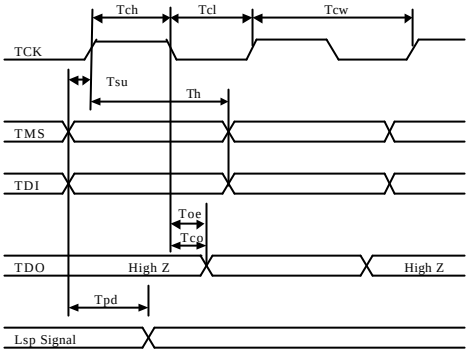
When PASS_THRU_ENABLE is "High" then the local scan ports are under control of the JTS03U device logic. When PASS_THRU_ENABLE is taken active (low) the if an invalid combination is presented on the PASS_THRU_SEL lines then all Local Scan Ports are Tri-Stated.

DC Requirements

The power requirements for the JTS03U device are minimal and are defined within the context of this datasheet

AC Requirements

Figure 2. JTS03U AC Timing Diagram



SYMBOL	Parameter	MIN	MAX	UNITS
Tcw	TCK clock pulse width	100	-	nS
Tch	TCK pulse width high	50	-	nS
Tcl	TCK pulse width low	50	-	nS
Tsu	TCK Setup time	30	-	nS
Th	TCK Hold time	40	-	nS
Toe	Neg Edge TCK to valid data enable	20	-	nS
Tco	Neg Edge TCK to valid data	15	-	nS
Tpd	Pass through Mode Primary / Lsp Delay	-	10	nS

JTS03U
IEEE1149.1 JTAG
3 Port Gateway

Absolute Maximum Ratings

Supply Voltage (Vcc) -0.3V to 5.5V

Vi = -0.5V -20mA
Vi = Vcc + 0.5V +20mA

DC Input Voltage (Vi) -0.5V to Vcc +0.5V

Input Current Iin :- 10uA

Max Junction Temperature with power applied Tj +125 degree C
Max Storage temperature –55 to +150 degrees C

Note. Stress above the stated maximum values may cause irreparable damage to the device, correct operation of the device at these values is not guaranteed

-

Recommended Operating Conditions

Supply Voltage (Vcc) JTSXX 3.0V to 3.6V

Input Voltage (Vi) 0V to Vcc

Output Voltage (Vo) 0V to Vcc

Operating Temperature(Ta)
Commercial 0 C to 70 C

Industrial (Ta) -40 deg C to +85 deg C 3.00V 3.6V

DC Electrical Characteristics

Symbol	Parameter	Max	Min	Units	Condition
V_{IH}	Minimum High Input Voltage	5.25	2.0	V	
V_{IL}	Maximum Low Input Voltage	0.8V	-0.3V	V	
Symbol	Parameter	Value		Units	Condition
V_{OH}	Minimum High Output Volotage	2.4V		V	Ioh=24mA or 8mA as defined by pin
V_{OL}	Minimum Low Output Voltage	0.4V		V	Iol=24mA or 8mA as defined by pin
I_{oz}	Tristate output leakage	-10 or 10 mA		mA	
I_{cc}	Maximum quiecennt supply current	2mA		mA	
I_{ccd}	Maximum dynamic supply current	80mA		mA	TCK freq equal to 10 Mhz

PIN NAME	PIN TYPE	LOC		Description	Stable signals states, with device unselected and active outputs on the device
LSP1_TCK	OUT	31	H4	IEEE1149.1 Test Clock on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH. Pin is PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 00, any other patterns then pin is TRI-STATE.	Buffered version of signal present on primary TCK
LSP1_TMS	OUT	32	J4	IEEE1149.1 Test Mode Select on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is 0 and PASS_THRU_SEL (1:0) signals are 00, any other patterns then pin is tri-state.	Logic '1'
LSP1_TDO	OUT	35	H5	IEEE1149.1 Test Data Out on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 00, any other patterns then pin is TRI-STATE.	Logic '1'
LSP1_TDI	IN	33	K4	IEEE1149.1 Test Data In on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 000, any other patterns then pin is TRI-STATE.	
LSP1_TRST	OUT	29	K3	IEEE1149.1 Test Reset on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 00, any other patterns then pin is TRI-STATE.	Buffered version of signal present on primary TRST
LSP1_AutoWR	OUT	30	J3	Flash, Memory Auto-Write on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL (1:0) signals are 00 PRIM_AutoWR is routed through to pin, any other patterns on PASS_THRU_SEL(1:0) pin is TRI-STATE.	Logic '1'
LSP1_DE	OUT	28	J2	PASS_THRU Debug Enable Output on Local Scan Port 1, active LOW when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 00 any other patterns on PASS_THRU_SEL(1:0) or PASS_THRU_ENABLE is HIGH then pin is HIGH.	Logic '1'
LSP2_TCK	OUT	41	J6	IEEE1149.1 Test Clock on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH. Pin is PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 01, any other patterns then pin is TRI-STATE.	Buffered version of signal present on primary TCK
LSP2_TMS	OUT	42	H6	IEEE1149.1 Test Mode Select on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is 0 and PASS_THRU_SEL (1:0) signals are 01, any other patterns then pin is tri-state.	Logic '1'
LSP2_TDO	OUT	45	J7	IEEE1149.1 Test Data Out on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 01, any other patterns then pin is TRI-STATE.	Logic '1'
LSP2_TDI	IN	44	K7	IEEE1149.1 Test Data In on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 01, any other patterns then pin is TRI-STATE.	
LSP2_TRST	OUT	37	K5	IEEE1149.1 Test Reset on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 01, any other patterns then pin is TRI-STATE.	Buffered version of signal present on primary TRST
LSP2_AutoWR	OUT	40	K6	Flash, Memory Auto-Write on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL (1:0) signals are 01 PRIM_AutoWR is routed through to pin, any other patterns on PASS_THRU_SEL(1:0) pin is TRI-STATE.	Logic '1'
LSP2_DE	OUT	36	J5	PASS_THRU Debug Enable Output on Local Scan Port 1, active LOW when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 01 any other patterns on PASS_THRU_SEL(1:0) or PASS_THRU_ENABLE is HIGH then pin is HIGH.	Logic '1'

PIN NAME	PIN TYPE	LOC 100 TQFP	LOC 100 cBGA	Description	Stable signals states, with device unselected and active outputs on the device
LSP3_TCK	OUT	49	K9	IEEE1149.1 Test Clock on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH. Pin is PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 10, any other patterns then pin is TRI-STATE.	Buffered version of signal present on primary TCK
LSP3_TMS	OUT	50	K10	IEEE1149.1 Test Mode Select on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is 0 and PASS_THRU_SEL (1:0) signals are 10, any other patterns then pin is tri-state.	Logic '1'
LSP3_TDO	OUT	53	H10	IEEE1149.1 Test Data Out on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 10, any other patterns then pin is TRI-STATE.	Logic '1'
LSP3_TDI	IN	52	J10	IEEE1149.1 Test Data In on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 10, any other patterns then pin is TRI-STATE.	
LSP3_TRST	OUT	47	J8	IEEE1149.1 Test Reset on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, PASS_THRU Output when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 10, any other patterns then pin is TRI-STATE.	Buffered version of signal present on primary TRST
LSP3_LSP_AutoWR	OUT	48	K8	Flash, Memory Auto-Write on Local Scan Port 1 when PASS_THRU_ENABLE is HIGH, when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL (1:0) signals are 10 PRIM_AutoWR is routed through to pin, any other patterns on PASS_THRU_SEL(1:0) pin is TRI-STATE.	Logic '1'
LSP3_DE	OUT	46	H7	PASS_THRU Debug Enable Output on Local Scan Port 1, active LOW when PASS_THRU_ENABLE is LOW and PASS_THRU_SEL(1:0) signals are 10 any other patterns on PASS_THRU_SEL(1:0) or PASS_THRU_ENABLE is HIGH then pin is HIGH.	Logic '1'
PRIM_TCK	IN	87	A6	IEEE1149.1 Primary Test Clock Input	
PRIM_TMS	IN	21	G2	IEEE1149.1 Primary Test Mode Select Input	
PRIM_TDO	OUT	20	G1	IEEE1149.1 Primary Test Data Output, TRI-STATE when JTS03is not selected.	HighZ
PRIM_TDI	IN	19	G3	IEEE1149.1 Primary Test Data Input	
PRIM_TRST	IN	22	H2	IEEE1149.1 Primary Test Reset Input, active LOW asynchronous reset of JTS03U, deselecting the JTS03U and placing the part in GOTOWAIT state	
PRIM_AutoWR	IN	16	F1	Primary Auto-Write Input controlled by test equipment to shorten Flash memory programming	
S(0)	IN	99	A2	JTS03U Slot Address(5:0) inputs, used to set address at which JTS03u will respond, typically set by hardwired connection on backplane.	
S(1)	IN	100	B2		
S(2)	IN	5	C2		
S(3)	IN	6	D3		
S(4)	IN	7	D1		
S(5)	IN	8	D2		

PIN NAME	PIN TYPE	LOC 100 TQP	LOC 100 cBGA	Description	Stable signals states, with device unselected and active outputs on the device
*TOE	IN	88	B6	Test Output Enable Input TRI-STATES all local scan ports, when taken to a logic low.	
LSP_RESET_n	IN	14	F4	Local Scan Port Reset input, active LOW resets JTS03U to GOTOWAIT and pulses all LSP TRST pins LOW to reset all devices with TRST function, typically this signal would be connected to a power on reset function.	
JTS03U_SELECTED	OUT	25	K1	JTS03U_selected Output, active LOW when JTS03U is selected, typically used to control off board buffering.	
LSP_ENABLE	OUT	24	J1	Local Scan Port enabled active LOW Output when JTS03U is selected and in level 1 protocol, typically used to set IEEE1149.1 compliance enable pins on devices	
USERCODE (15:0)	IN	64,65,67,68,69,70,71,72,75,76,77,78,79,80,81,83 (MSB-LSB)	E9,E10,E8,E7,D9,D10,D8,C9,C10,B10,B9,A9,A8,B8,A7,B7 (MSB-LSB)	JTS03U User/Board identification inputs (15:0), used to establish board type and revision so as to ensure correct IEEE1149.1 test vector sets are applied	
USR_STATUS_BYTE(7:0)	IN	84, 85, 92, 93, 94, 96, 97, 98 (MSB-LSB)	C7,C6,C5,C4,B4,A4,B3,A3 (MSB-LSB)	JTS03U Status Byte inputs (7:0), are used to provide status information of the PCB under test back to the test master via the IEEE1149.1 bus ie:- Eight signals levels can be monitored and then reported via the IEEE1149.1 bus in a non intrusive manner.	
SELF_TEST	OUT	27	K2	Provides a low going pulse under command from the IEEE1149.1 bus which can be used to start self test functions on a PCB	Logic '1'
PASS_THRU_Enable	IN	9	E4	PASS_THRU enable Input active HIGH disables PASS_THRU function, active LOW enables PASS_THRU mode.	
PASS_THRU_SEL(1:0)	IN	12,10 (HSB-LSB)	E1,E3 (HSB-LSB)	JTS03 PASS_THRU select inputs (2:0), used to select active routing of PASS_THRU port enabled by active LOW on PASS_THRU_Enable pin. 00 = LSP1, 01 = LSP2, 10 = LSP3	
GND	POWER	38, 86, 11, 26, 43, 59, 74, 95, 2, 17, 54, 56 , 90	D6, G5, C3, D7, E5, F6, G4,H8,A5, B1, F2, H9, G9	JTS03U Ground connection	
VCC	POWER	39, 91, 3, 18, 34, 51, 66, 82,23,55	D5, G6, C8, D4, E6, F5, G7, H3,H1,J9	JTS03U VCC connection	
ASIC_TEST_EN	No Connect	89	B5	Factory test enable pin, this pin should be left un connected when the ASIC is fitted.	

PIN NAME	PIN TYPE	LOC		Description	Stable signals states, with device unselected and active outputs on the device
ASIC_TCK	IN	62	F8	IEEE1149.1 ASIC Test Clock Input	
ASIC_TMS	IN	15	F3	IEEE1149.1 ASIC Test Mode Select Input	
ASIC_TDO	OUT	73	A10	IEEE1149.1 ASIC Test Clock Output	
ASIC_TDI	IN	4	A1	IEEE1149.1 ASIC Test Clock Input	
No Connects		1,13,63,61,60,58,57	C1,E2,F7,F10,F9,G8,G10		

Mechanical Requirements

This is a 100 pin plastic TQFP (Thin Quad Flat Pack) package

Leadframe Plating: Copper base material with a 5-micron (200 micro-inches) minimum of Tin/Lead overplating containing 10 - 40% lead.

Terminations:

Coplanarity (from component seating plane): 0.1 mm (0.004 inches) max.

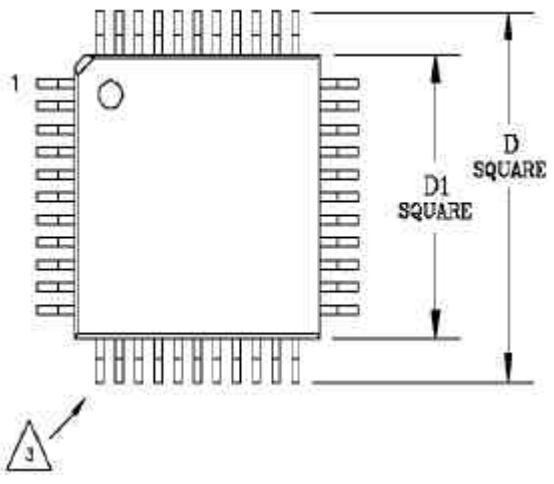
Seating plane is the plane established by the contact points of three or more leads that support the part when it is placed on top of a planar surface. Deviation from coplanarity is the distance between the intended contact point of a lead and the established seating plane per JESD22-B108.

Lead Skew: Perpendicularly of the lead rows with respect to reference axes created by the center leads of each row to be within 0.05 mm (0.002 inches). Also, the lead position is to be within 0.2 mm (0.008 inches) with respect to the reference axis.

Leaded Parts shall comply with the test method appropriate to this part in JESD22-B102,

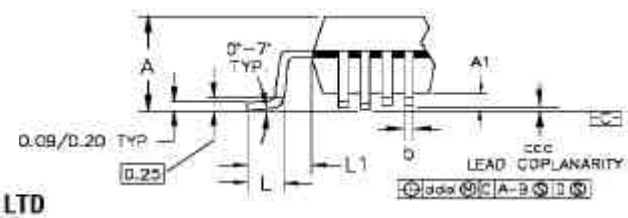
Solderability Test Method.

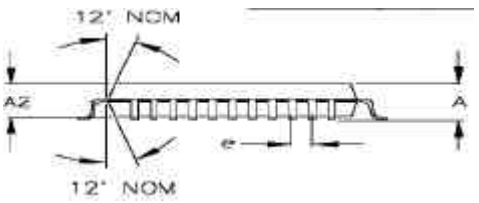
IC Package Configuration:



SYMBOL	LEADS / TOL.	100 LEAD
A	MAX.	1.60
A_1	MIN / MAX	0.05 / 0.15
A_2	NOM / NOM / MAX	1.35 / 1.40 / 1.45
D	BASIC	16.00
D_1	BASIC	14.00
L	±0.15	0.60
L1	REF	1.00
b	MIN / MAX	0.17 / 0.27
e	BASIC	0.50
ccc	MAX	0.08
ddd	NOM	0.08
JEDEC REF #		MS-026

NOTES
1. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
2. PLASTIC BODY DIMENSIONS DO NOT INCLUDE FLASH OR PROTRUSION. MAX ALLOWABLE 0.25 PER SIDE.
3. LEAD COUNT ON DRAWING NOT REPRESENTATIVE OF ACTUAL PACKAGE.





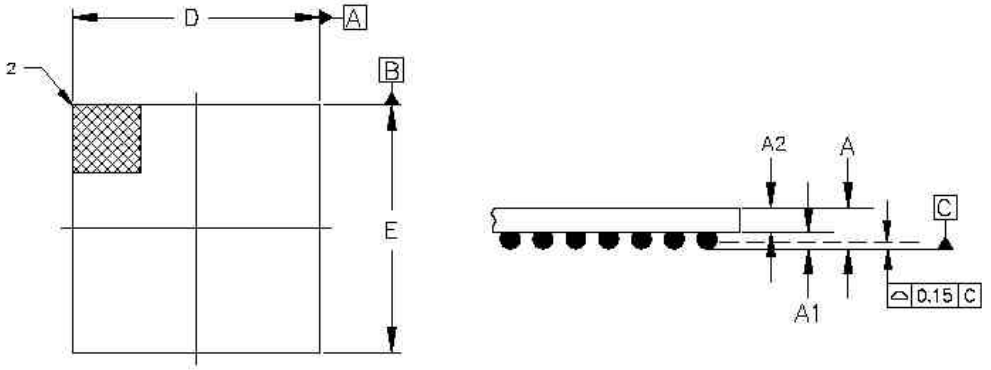
BGA Package information

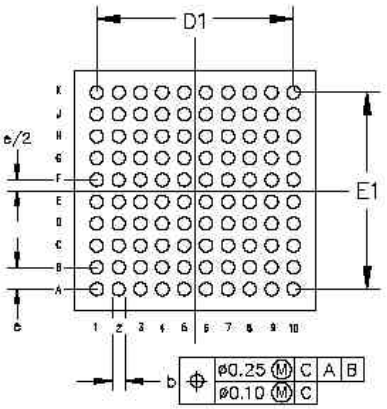
Mechanical Requirements

This is a 100 pin plastic cBGA (Ball gride array) package

Leaded Parts shall comply with the test method appropriate to this part in JESD22-B102, Solderability Test Method.

IC Package Configuration:





DIMENSIONS			
SYMBOL	MIN	NOM	MAX
A	--	--	1.70
A1	0.30	--	--
A2	0.25	--	1.10
b	0.60	0.60	0.70
D	11.00 BSC		
D1	9.00 BSC		
E	11.00 BSC		
E1	9.00 BSC		
e	1.00		
PACKAGE NUMBER	FBGA0100-11F		
JEDEC REF #	MO-192 VAR. AAC-1		

NOTES:
1. ALL LINEAR DIMENSIONS ARE IN MILLIMETERS.
2. DETAILS OF A1 CORNER MAY OPTIONAL, MAY BE ONE OF THE CUT, LASER MARK OR MOLDED MARKING, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED.

Device Selector Guide

JTS XX X – XX XXXX X

Product identifier

Device Family

01: Controller
02: Sequencer
03: 3 Port Gateway
06: 6 Port Gateway
08: 6 port & Sequencer
10: 6 port & Controller

Product Version

S = Standard
U = 16 bit user code
Bu= 8 bit status/user code
E = Enhanced

TCK speed

10= 10 MHZ TCK

Package

T100=100 pin TQFP
f49= cBGA 49 pin
F144 = fPBGA144 pin
F100=fBGA100pin
F256 = fPBGA256 pin

Grade

G: RoHS 6/6
Blank =Commercial
I = Industrial

Device Master	Description	Package Options				
		49CBGA	100 cBGA (1mm pitch)	100 TQFP	144 cBGA (1mm pitch)	256 fBGA (1mm pitch)
JTS01	Controller	P	x	x		
JTS02	Sequencer		x	x		
JTS03S	3 Port Gateway (No User-code or Status register)	P	x	x		
JTS03U	3 Port Gateway (16 bit usercode)		x	x		
JTS03E	3 Port Gateway (Enhanced)				x	x
JTS04E	3 Port Gateway (Enhanced) + Controller					x
JTS04S	3 port Gateway (no user code no status) + Control-er		x	x		
JTS06S	6 Port Gateway (No User-code or Status register)		x	x		
JTS06BU	6 Port Gateway (8 bit status/usercode)		x	x		
JTS06E	6 Port Gateway (Enhanced)				x	x
JTS07	3 Port Gateway (enhanced) + sequencer				x	
JTS08	6 Port Gateway + Se-quencer					x
JTS10	6 Port Gateway + Controller					x
JTS10U	3 Port Gateway (16 bit usercode) + Controller				x	

X: available P: planned

JTS03U
IEEE1149.1 JTAG
Gateway

Disclaimer:

Firecron's products are not authorized for use as critical components in life support devices or systems without the express written approval of the company. As used herein:

Life support devices or systems are devices or sy stems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, whose failure to perform when properly used in accordance with the instructions for use provided in the labelling can be reasonably expected to result in a significant injury to the user

A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness

Firecron does not accept any responsibility for any circuitry described. Firecron reserves the right at any time without notice to change the data , circuitry and specification

Firecron LTD
Technology Solutions

The Leader in IEEE 1149.1 Design for Test Solutions